REMARKS

This is an amendment under 37 CFR §1.116. The amendments and remarks herein, to the extent they were not presented earlier, are now presented because they are necessitated by the arguments made by the Examiner in the last office action. It is submitted that these amendments do not raise new issues and do not require any further searching. Since this amendment is being filed within two months of the mailing date of the final rejection, an advisory action is respectfully requested. Claims 1-4, 7-8, 10, 12, 16-19, and 22-30 are in this application. Claims 5-6, 9, 11, 13-15, and 20-21 have been cancelled. Claim 22 has been amended.

The Examiner rejected claims 1-3, 16-17, 21, and 26 under 35 U.S.C. §102(b) as being anticipated by, or in the alternative under 35 U.S.C. §103(a) as being unpatentable over, Larson et al. (U.S. Patent No. 5,481,680). As noted above, claim 21 has been cancelled. For the reasons set forth below, applicant respectfully traverses the rejections of claims 1-3, 16-17, and 26.

With respect to claims 1 and 16, in the amendment filed on May 15, 2006, applicant noted that claims 1 and 16 can not be anticipated by Larson because Larson fails to teach or suggest that a number of first addresses are assigned to a group of devices such that two or more consecutive first addresses are assigned to each device in the group.

In rejecting claim 1, the Examiner acknowledged that the Larson reference does not disclose that a number of first addresses are assigned to a group of devices such that two or more consecutive first addresses are assigned to each device in the group. In rejecting claim 16, the Examiner appears to indicate that the limitation that the logic circuit assign a number of first addresses to the group of devices such that two or more consecutive first addresses are assigned to each device in the group was rejected as in claim 1.

Thus, since the Examiner acknowledged that Larson does not disclose that a number of first addresses are assigned to a group of devices such that two or more consecutive first addresses are assigned to each device in the group, claims 1 and 16 are not anticipated by the Larson reference. In addition, since claims 2-3 and 17 depend either directly or indirectly from claims 1 and 16, respectively, claims 2-3 and 17 are not anticipated by the Larson reference for the same reasons that claims 1 and 16, respectively, are not anticipated by the Larson reference.

In further rejecting claim 1, the Examiner also pointed to column 5, lines 47-50 of Larson as teaching that, although the block of memory illustrated in FIG. 7 contains a simple priority grant algorithm, the block of memory is not required to contain the priority scheme shown in FIG. 7. In view of this text, the Examiner argued that Larson teaches that any other arbitration scheme can be used, including one where a number of first addresses are assigned to a group of devices such that two or more consecutive first addresses are assigned to each device in the group and no two devices have the same first address.

Applicant notes, however, that the mere teaching that other arbitration schemes can be used does not render obvious every other conceivable arbitration scheme. The logical extension of the Examiner's argument is that it is impossible to ever invent another arbitration scheme because all conceivable arbitration schemes are obvious in view of Larson's teaching that another arbitration scheme can be used.

In addition, to establish a prima facia case of obviousness, there must be some objective teaching in Larson (or knowledge generally held by one of ordinary skill in the art) that would motivate one skilled in the art to incorporate into Larson a scheme where a number of first addresses are assigned to a group of devices such that two or more consecutive first addresses are assigned to each device in the group and no two devices have the same first address.

In the present rejection, the Examiner has not pointed to any discussion in Larson that teaches or suggests incorporating a scheme where a number of first addresses are assigned to a group of devices such that two or more consecutive first addresses are assigned to each device in the group and no two devices have the same first address. As a result, the Examiner has not established a prima facia case of obviousness.

Thus, since a teaching that other approaches can be used does not render obvious every other conceivable approach, and the Examiner has not established a prima facia case of obviousness, claims 1 and 16 are patentable over Larson. In addition, since claims 2-3 and 17 depend either directly or indirectly from claims 1 and 16, respectively, claims 2-3 and 17 are patentable over Larson for the same reasons that claims 1 and 16, respectively, are patentable over Larson.

With respect to claim 26, in the amendment filed on May 15, 2006, applicant noted that claim 26 is not anticipated by Larson because Larson fails to teach or suggest that no two second addresses are identical. In the present office action, the Examiner indicated that claim 26 was rejected on the same rationale and arguments as the rejection of claim 1.

In the present rejection of claim 1, the Examiner pointed to the rows of addresses shown in the left column of FIG. 7 of the Larson reference as constituting the first addresses required by the claims, and appears to point to the rows of grant bits G0-G3 shown in FIG. 7 of Larson as constituting the second addresses required by the claims.

In the amendment filed on May 15, 2006, applicant noted that FIG. 7 of the Larson reference teaches that the contents of grant bit rows 2, 4, 6, 8, 10, 12, 14, and 16 are identical, each having the value of 0001. Thus, rather than teaching that no two rows of grant bits are identical, Larson instead teaches that a number of the rows of grant bits are identical. Therefore, since Larson fails to

teach or suggest that no two rows of grant bits are identical, the rows of grant bits can not be read to be the second addresses required by claim 26.

However, from what can be determined, the Examiner did not address this argument in the present rejection of claim 1. As a result, claims 26-30 are not anticipated by Larson. In addition, the Examiner has not pointed to any discussion in Larson that teaches or suggests forming rows of grant bits where no two rows of grant bits are identical. As a result, the Examiner has not established a prima facia case of obviousness. Thus, since the Examiner has not established a prima facia case of obviousness, claims 26-30 are patentable over Larson.

The Examiner objected to claims 4, 7-8, 10, 12, 18-19, 22-25, and 27-30, but indicated that these claims would be allowable if rewritten in independent form to include all of the limitations of the base claim and any intervening claims. Claim 22 has been amended to be in independent format. Claims 23-25 have not been amended to be in independent format as these claims depend from claim 21. Further, in view of the above discussion, claims 4, 7-8, 10, 12, 18-19, and 27-30 have not been amended to be in independent form.

Thus, for the foregoing reasons, it is submitted that all of the claims are in a condition for allowance. Therefore, the Examiner's early re-examination and reconsideration are respectively requested.

Respectfully submitted,

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